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EXAMINER	
SORRELL, ERON J	
ART UNIT	**PAPER NUMBER**
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/494,787	MOUNT, JOHN A.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-14* is/are allowed.

6)☒ Claim(s) *1-5 and 15-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

1. In view of the Appeal Brief filed on 5/2/07, PROSECUTION IS HEREBY REOPENED. New grounds of rejections are set forth below. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

Allowable Subject Matter

2. The indicated allowability of claim 15 is withdrawn Rejections based on the cited prior art reference(s) follow.

3. Claims 6-14 remain allowed.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: item 350 in figure 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-5 and 15-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Independent claims 1,16, and 21 recite the use of "a bus" to both transfer data and to update registers. This limitation of using a single bus to perform both actions does not appear to be supported by the original specification. Applicant's figure 3 and associated description at page 8, lines 5-23, appear to disclose the use of more than one bus for performing both actions. Data is read from the disk stack 500. Disk stack 500 is coupled to E-block 400 which houses the read heads that read the data from the disk stack 500. E-block 400 has an interface 450, which is described in the specification as being "intelligent" and may comprise a pre-amp chip. The interface 450 is coupled to the read heads via bi-directional communication lines. ***Data read from the disk stack must go through these bi-directional communication links in order to get***

to the PCBA 600. These bi-directional communication links are buses. PCBA has a bus 360 that performs the updating of the registers in the slave IC 300, this bus also transfers data from the disk stack after it has been transferred over the bus connecting the interface 450 to the read heads. Therefore, the use of one bus to perform both the register updating and data reading is not enabled by the specification.

7. Dependent claims 4-5, 17-20, and 22-25 are rejected based on there dependency to the independent claims rejected above.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-5 and 15-25 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. In light of the 112-1st paragraph rejection above, it is unclear how the limitation of "the bus" is supposed to be interpreted, in light of the specification. As best understood

by the Examiner, the term bus as used by the applicant is being construed as a collection of bus segments coupling different parts, but not necessarily all of the parts, of the system.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1,2,3,5,16,18, and 19, are rejected under 35 U.S.C. 102(b) as being anticipated by Hessing et al. (U.S. 5,276,564 hereinafter "Hessing").

13. Referring to claim 1, Hessing teaches in an apparatus (fig. 1) having a bus (see all signal lines connecting items 12,20, and 26, note the bus comprises all of the connecting signal lines) operatively coupled to a first controller chip (see item 26 in figure 1) and a first channel chip (see item 20 in figure 1), the channel chip having several registers (fig. 2), the storage system also having a storage medium (see lines 38-57 of column 2) operatively coupled to the bus through a storage medium interface (see item 12 in figure 1), a method for retrieving data recorded on the storage medium comprising the step of:

(a) retrieving a first portion of the record data via the bus (see lines 24-47 of column 5);

(b) updating some of the registers via the bus (see lines 49-67 of column 5); and

(c) retrieving a second portion of the record data via the bus (see lines 24-47 of column 5).

14. Referring to claim 2, Hessing teaches in interface includes a read head, further comprising a step (d) of repositioning the storage medium interface with respect to the storage medium, between retrieving steps (a) and (c) (see lines 38-57 of column 2).

15. Referring to claim 3, Hessing teaches the interface has a plurality of operating parameters that are modified in the updating step (see lines 11-19 of column 2, note the interface can transfer data or servo data).

16. Referring to claim 5, Hessing the registers contain at least one mode-indicating value (see lines 49-67 of column 5, note either the data mode or servo mode is in operation).

17. Referring to claims 16 and 21, Hessing teaches a method comprising:

providing data via a bus (see lines 24-47 of column 5, see all signal lines connecting items 12,20, and 26, note the bus comprises all of the connecting signal lines);

updating at least one register or parameter via the bus (see lines 49-67 of column 5); and

providing data via the bus responsive to the updating (see lines 24-47 of column 5).

18. Referring to claims 18 and 22, Hessing teaches the bus is parallel (see all signal lines connecting items 12,20, and 26, note the bus comprises all of the connecting signal lines).

19. Referring to claim 19, Hessing teaches the steps are controlled by a processor (see lines 48-67 of column 3).

20. Referring to claim 23, Hessing teaches the first and second data are respectively characterized as user data transferred between a host device and a storage medium (see lines 11-19 of column 3).

21. Referring to claim 24, Hessing teaches the user data are transmitted via the bus between a read/write channel (item 12, figure 1) and a controller (item 26, figure 1).

22. Referring to claim 25, wherein the first data are transmitted at a first data rate and the second data are transmitted at a second rate different than the first rate (see lines 1-13 of column 2).

23. Claims 16,18,19,21, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Goodrum (U.S. Patent No. 6,260,095).

24. Referring to claims 16 and 21, Goodrum teaches a method comprising:

providing data via a bus (see lines 53-55 of column 2);

updating at least one register or parameter via the bus (see lines 53-55 of column 2, note since the write posting buffer receives new up to date data, the buffer "updated"); and

providing data via the bus responsive to the updating (see lines 53-55 of column 2, note the acknowledgment is the second data).

25. Referring to claim 18 and 22, Goodrum teaches the bus is a parallel bus (see item 110 in figure 1A, note the primary bus is a processor bus).

26. Referring to claim 19, Goodrum teaches the steps are performed by a processor (see item 102 in figure 1A, note the CPU controls the writing to the bus bridge).

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hessing in view of Du et al. (U.S. Patent No. 6,381,085 hereinafter "Du").

29. Referring to claim 4, Hessing fails to teach the registers contain at least one read channel parameter value selected from the group consisting of: a precompensation value, a filter coefficient value, and a phase offset value.

Du teaches in an analogous system, registers containing a read channel parameters comprising at least a filter coefficient value (see lines 21-35 of column 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system and method of Hessing with the above limitation of Du. One of ordinary skill in the art would have been motivated to make such modification because Du suggests this parameter helps improve the bit error rate (see lines 21-35 of column 2).

30. Claims 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hessing in view of O'Brien et al. (U.S. Patent No. 3,883,853 hereinafter "O'Brien").

31. Referring to claim 17, Hessing fails to teach the bus is a serial bus. O'Brien teaches, in an analogous system, the bus being a serial bus (see data bus in figure 3).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Hessing such that the bus is a serial bus to reduce the overall cost of the system.

32. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hessing in view of Taniai et al. (U.S. Patent No. 5,438,665 hereinafter "Taniai").

33. Referring to claim 15, Hessing teaches an apparatus comprising:

an interface configured to read data from a storage medium (see item 12 in figure 1);

a memory containing several values indexed by zone identifiers (see lines 36-43 of column 1);

a first controller chip containing a microprocessor (see item 26 in figure 1);

a first channel chip having several registers (see item 20 in figure 1);

and a bus (see lines 24-47 of column 5, see all signal lines connecting items 12,20, and 26, note the bus comprises all of the connecting signal lines) operatively coupled between the interface and the chips.

Hessing fails to teach the controller chip having direct memory access (DMA) controller, the DMA controller operatively coupled to the memory.

Taniai teaches a DMA controller that provides data via a bus, updates registers via a bus, and provides data via the bus responsive to the update (see lines 6-32 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Hessing with the above teachings of Taniai. One of ordinary skill in the art would have been motivated to make such modification in order to relieve the processor of the burdensome task of transferring data.

34. Referring to claim 20, Hessing teaches the method of claim 16, as shown above, however fails to teach the steps are

performed by a DMA controller. Taniai teaches a DMA controller that provides data via a bus, updates registers via a bus, and provides data via the bus responsive to the update (see lines 6-32 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Hessing with the above teachings of Taniai. One of ordinary skill in the art would have been motivated to make such modification in order to relieve the processor of the burdensome task of transferring data.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJS
August 28, 2007

KIM HUYNH
SUPERVISORY PATENT EXAMINER

9/4/07